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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/063,128	03/25/2002	Chao-Hu Liang	NAUP0385USA	5968

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EXAMINER	
MAI, ANH D	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 09/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/063,128	LIANG ET AL.	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Status of the Claims

1. Amendment filed July 4, 2003 has been entered as Paper No. 3. Claims 1, 2, 4, 8, 9 and 16 have been amended. Claims 1-17 are pending.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-8 and 17 are rejected under 35 U.S.C. 112, second paragraph, as failing to set forth the subject matter which applicant(s) regard as their invention. Evidence that claims 1-8 and 17 fail(s) to correspond in scope with that which applicant(s) regard as the invention can be found in specification originally filed March 25, 2002. In that paper, applicant has stated "contaminants adhering to the semiconductor wafer 100 **are removed**" (see [0025]); "the present invention shows marked improvement in **preventing the occurrence of particles and defects** of various shapes and sizes" (see [0030]), and this statement indicates that the invention is different from what is defined in the claim(s) because claim 1 recites: "the surface of the semiconductor wafer **comprising a plurality of particles**" (lines 2-3).

3. Claims 1-8 and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites: "the surface of the semiconductor wafer **comprising a plurality of particles**" (lines 2-3)".

Please note: prior to performing two-step deposit, the semiconductor wafer have been cleaned by: megasonic scrubbing, SC-1 and SC-2 clean. ([0025]). Therefore, all particles (contaminants adhering the semiconductor wafer; organic contaminants and particles and metallic contaminants) have been removed. (See [0025]).

Therefore, the preamble of claim 1 clearly lacks support from the specification.

Where are those "plurality of particles" came from since the wafer have been thoroughly clean ?

With respect to claim 5, Applicant asserted that "the term particles means the already existing particles on the surface of the semiconductor wafer before performing the two-step silicon deposition process".

As clearly discussed above, prior to the two-step deposition, the semiconductor wafer has been thoroughly wet cleaned (megasonic, SC-1 and SC-2) to remove the particles. ([0025]).

With respect to claim 17, the limitation of claim 17 includes: wherein the defects comprises needle-like defects".

While claim 9, which claim 17 depends-on, recites: "wherein the two-step silicon deposition process comprises a first step low temperature amorphous silicon (α-Si) deposition process **to avoid formation of particles and defects by inhibiting nucleation**...".

Therefore, claim 17 is contrary to claim 9, because the formation of the defects have been avoided by the formation of the amorphous silicon layer.

What is the shape of the particles that does not exist ?

Please note: the needle-like defects only exists if the amorphous silicon have not been formed. (See Fig. 6, page 4, [0013-0014]).

Claim Rejections - 35 USC § 102

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1, 7 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Balasubramanian et al. (U.S. Patent No. 5,767,004) of record.

With respect to claim 1, as best understood by the examiner, Balasubramanian teaches a method for making a polysilicon film on a semiconductor wafer, the method comprising:

performing a two-step silicon deposition process, the two-step silicon deposition process comprising:

a first step amorphous silicon (16) deposition process utilizing a low temperature; and

a second step polysilicon (18) deposition process utilizing a high temperature. (See Fig. 1, col. 1-12).

With respect to the functional limitation of the two-step deposition process: "wherein the first step amorphous silicon (α-Si) deposition process is used to avoid nucleation of the polysilicon film growth, which growing by way of the particles on the surface of the semiconductor wafer, so as to inhibit occurrences of needlelike particles and defects on the surface of the polysilicon film", since the deposition process of Balasubramanian is performed by two-steps silicon deposition as claimed, thus "avoiding nucleation of the polysilicon film growth, which growing by way of the particles on the surface of the semiconductor wafer so as to inhibit occurrences of needlelike particles and defects on the surface of the polysilicon film" is an inherent result of the two-steps silicon deposition.

With respect to claim 7, the polysilicon layer (18) of Balasubramanian is deposited at the temperature that includes the claimed range.

With respect to claim 8, the two-step silicon deposition process of Balasubramanian is performed in single wafer type LPCVD equipment.

Note that, until proven otherwise, the LPCVD equipment of Balasubramanian includes single wafer type LPCVD equipment.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Balasubramanian '004 as applied to claim 1 above, and further in view of Yu et al. (U.S. Patent No. 6,225,167) of record.

With respect to claim 2, Balasubramanian teaches a method of making a polysilicon film on a semiconductor wafer including defining the active area, growing gate oxide and performing a two-step silicon deposition process. (See col. 5, line 59-col. 6, line 13).

Thus, Balasubramanian is shown to teach all the features of the claim with the exception of explicitly disclosing the process performed prior to the two-step silicon deposition process.

However, Yu teaches the process performed prior to depositing conductive gate electrodes includes: at least one photolithography process, one wet etching process, one photoresist stripping process, one wet cleaning process and one thermal oxidation process are performed on the surface of the semiconductor wafer (200).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the polysilicon film on the semiconductor wafer of Balasubramanian by performing the pre-deposition processes as taught by Yu to define the active area and to form the gate oxide for the silicon gate electrodes.

With respect to claim 3, the wet etching process of Yu comprises a buffer oxide etchant (BOE) etching process and followed by a SC-1 cleaning process.

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Balasubramanian '004.

Balasubramanian teaches the first step amorphous (16) is deposited at a temperature range (500 to 580 °C) that overlaps the claimed range (550 to 650 °C) and at a thickness of about 400 Å.

Thus, Balasubramanian is shown to teach all the features of the claim with the exception of explicitly forming a thinner amorphous layer (100 Å). Note that, the claimed thickness does not appear to be critical.

Note that the specification contains no disclosure of either the *critical nature of the claimed thickness, 100 Å, of any unexpected results arising therefrom.* Where patentability is aid to based upon particular chosen dimension or upon another variable recited in a claim, the Applicant must show that the chosen dimension are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the amorphous silicon film of Balasubramanian to a thickness that able to create a grain boundary mis-matched, thus, forming a low impurity diffusion gate electrode.

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Balasubramanian '004 as applied to claim 1 above, and further in view of Applicant admitted prior art.

As best understood by the examiner, Balasubramanian is shown to teach all the features of the claim with the exception of disclosing any contaminants if existed prior to the deposit of the amorphous silicon layer (16).

However, the admitted prior art teaches that there are many contaminants exited in a semiconductor process including: particles, organic substance, micro-defects and metal particles adhering to the wafer. (See [0006]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to includes the particles in the semiconductor wafer of Balasubramanian as taught by the admitted prior art because the particles should not be detrimental to the process since they would have been removed by the wet cleaning process.

8. Claims 9-12 and 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu '167 in view of Balasubramanian '004.

Yu teaches a method for forming a polysilicon film on a semiconductor wafer, a surface of the semiconductor wafer comprising a first gate oxide area (40) and a second gate oxide area (50), substantially as claimed including:

forming a first gate oxide layer (20) on the surface of the semiconductor wafer (10);

performing a photolithography process and an etching process to remove the first gate oxide layer (20) on the surface of the second gate oxide area (50);

performing a cleaning process; and performing a conductive gate electrodes deposition process covering the first gate oxide area (40) and the second gate oxide area (50) to form MOS transistors. (See Fig. 1a-d, col. 1-10).

Thus, Yu is shown to teach all the features of the claim with the exception of explicitly disclosing the process of forming the conductive gate electrodes.

However, Balasubramanian teaches a process of forming conductive gate electrodes covering gate oxide including:

performing a two-step silicon deposition process to form a polysilicon layer (18), the polysilicon layer (18) covering the gate oxide layer (14), wherein the lower layer (16) of amorphous silicon is deposited at a low temperature and the upper layer (18) of polysilicon is deposited at a high temperature. (See Fig. 1, col. 6, lines 33-67).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the conductive gate electrodes of Yu using the two-step silicon deposition process as taught by Balasubramanian to form a low impurity diffusion polysilicon layer within an integrated circuit. (See col. 3, lines 6-8).

Regarding the functional limitation: "wherein the two-step silicon deposition process comprises a first step low temperature amorphous silicon deposition process to avoid formation of particles and defects by inhibiting nucleation during the formation of the polysilicon layer, and a second step high temperature polysilicon deposition process", since the two-step deposition of Balasubramanian includes depositing an amorphous silicon (16) on a gate oxide layer (14) at a low temperature, thus, the formation of the amorphous silicon layer (16) of Balasubramanian is inherently result in avoiding the formation of particles and defects by inhibiting nucleation during the formation of the polysilicon layer (18).

With respect to claim 10, the etching process of Yu is a wet etching process.

With respect to claim 11, the wet etching process of Yu utilizes a buffer oxide etchant (BOE).

With respect to claim 12, the cleaning process of Yu is a wet cleaning process.

With respect to claims 14 and 15, the temperature ranges of the first step low temperature of amorphous silicon (16) deposition process and second step high temperature polysilicon (18) deposition process of Balasubramanian overlaps the claimed range. (See col. 6, lines 33-67).

With respect to claim 16, the two-step silicon deposition process of Balasubramanian is performed in single wafer type LPCVD equipment. (See col. 11, lines 16-20).

With respect to claim 17, as best understood by the examiner, Yu is shown to teach all the features of the claim with the exception of disclosing the defects includes needle-like defects.

However, in view of Balasubramanian, the two-step deposit of the silicon electrode including deposit amorphous silicon layer (16) on the gate oxide (14) prior to deposit polysilicon layer (18) is inherently result in avoiding formation of particles defects.

9. Claims 4 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Balasubramanian '004 and Yu '167 as applied to claims 2 and 9 above, and further in view of Hayakawa (U.S. Patent No. 5,779,520) of record.

Balasubramanian '004 and Yu '167 teach a wet cleaning process utilizing RCA clean. Note that RCA cleaning comprises SC-1 and SC-2.

Thus, Balasubramanian '004 and Yu '167 are shown to teach all the features of the claim with the exception of further utilizing megasonic scrubbing.

However, Hayakawa teaches: cleaning is more effective with physical scrubbing including megasonic scrubbing. (See col. 2, lines 56-63).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to combine RCA cleaning of Yu with megasonic scrubbing as taught by Hayakawa for utmost effective in removing contaminants.

Response to Arguments

10. Applicant's arguments filed July 4, 2003 have been fully considered but they are not persuasive.

With respect to claim 1, contrary to Applicant assertion, the amended claim does not overcome the rejection as indicated.

In response to applicant's argument that "the first step amorphous silicon deposition process **is used to** avoid nucleation of the polysilicon film growth, ...so as to inhibit occurrences of needle-like particles and defects on the surface of the polysilicon film", a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

Since the process of Balasubramanian includes depositing the amorphous silicon layer prior to the deposition of the polysilicon layer, the nucleation of the polysilicon film growth is

inherently resulted. Further, Applicants clearly indicated that "preventing the occurrence of particles and defects" is achieved by the formation of the α-Si, not the cleaning process.

The process of Balasubramanian anticipates the amended claim.

With respect to claims 9, contrary to Applicant believes, the amended claim is obvious over the teaching of Yu and Balasubramanian.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (703) 305-0575. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

A.M
August 25, 2003

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800